WHAT IS CLAIMED IS:

1. A microprocessor for executing instructions obtained from an instruction store, said microprocessor comprising:

a) means for fetching instruction sets from an instruction store, each instruction set including an instruction;

b) means, coupled to said fetching means, for buffering instruction sets, said buffering means including a first buffer and a second buffer; and

c) means, coupled to said first and second buffers, for executing instructions, said executing means including register file means for storing data in a plurality of registers, a plurality of functional unit means for processing data wherein each said functional unit means processes data in a predetermined manner, bus means for providing plural data routing paths between said register file means and said plurality of functional unit means, and means for controlling the execution of instructions.

2. The microprocessor of claim 1 wherein said controlling means is coupled to said first and second buffers for examining the instructions within the instruction sets buffered therein, said controlling means including means for selecting an instruction to be executed, means for selecting instruction determined ones of said plurality of registers for the transfer of data and instruction determined ones of said plurality of functional unit means for the processing of data.

3. The microprocessor of claim 2 wherein said controlling means directs the operation of said bus means to transfer data between said instruction determined one of said plurality of registers and said instruction determined ones of said plurality of functional unit means.

4. The microprocessor of claim 1, 2, or 3 wherein said controlling means provides for the concurrent execution of instructions, said controlling means controlling the initiation of the execution of instructions based on the availability of said functional unit means for the processing of data.

5. A microprocessor comprising:

a) means for obtaining a predetermined sequence of instructions to be executed, wherein an instruction of said predetermined sequence of instructions includes a register reference;

b) means for storing respective data in a plurality of registers including a predetermined register and a temporary register; and

c) means, coupled to said obtaining means, for sequentially executing said predetermined sequence of instructions, said executing means including means for directing the storage of data by an a-sequentially executed instruction to said temporary register where the register referenced by said a-sequentially executed instruction is said predetermined register.

6. A microprocessor comprising:

a) means for storing data in a plurality of registers identifiable by register references, said plurality of registers including a predetermined register and a temporary register;

b) means for obtaining a predetermined sequence of instructions to be executed, wherein an instruction of said predetermined sequence of instructions includes a register reference;

c) executing means, coupled to said obtaining means, for a-sequentially executing said predetermined sequence of instructions, said executing means including means, coupled to said storing means, for selecting saied temporary register where the sequential execution of said instruction provides said register reference to select said predetermined register for the storage of data.

7. The microprocessor of claim 6 wherein said executing means further includes means for determining whether all instructions in said predetermined sequence of instructions prior to said instruction have been executed and means, responsive to said determining means and coupled to said storing means, for transferring the data stored by said temporary register to said predetermined register.